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EXAMINER	
MAGEE, THOMAS J	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 04/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/785,345	GLIDDEN ET AL.	
	Examiner	Art Unit	
	Thomas J. Magee	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-28 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-28 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections – 35 U.S.C. 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office Action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1 – 6, 8 – 14, 16, 17, 19, 22, 23, and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Farnworth et al. (US 6,020,629) in view of Hitachi Chemical Co., ("Epoxy Molding Compounds," 2003) and Pace (US 6,165,820)..

3. Regarding Claims 1 – 3, 10 and 11, Farnworth et al. disclose a packaged solid state assembly comprising:

a first ceramic substrate (12) (Figure 2A) (Col. 3, lines 59 – 61) and a second ceramic substrate (12A) (Col. 5, lines 12 – 14) and at least one solid state device (20) (upper) located therebetween, each solid state device comprising a body having a coefficient of thermal expansion and a plurality of conductive contacts (34) on a surface of the body facing the second ceramic substrate (12A),

the first ceramic substrate comprising:

a body with a lower side and an upper side facing the solid state devices (upper),

a conductive pad (48) (Figures 2A, 2D) covering the lower side, and

one conductive pad (38) (Figures 2C, 2D) connected to each of the solid

state devices packaged, each conductive pad (38) being bonded to the upper side of the body and connected to the solid state device with which it is associated, each pad being separated from other metal pads by a distance sufficient to prevent breakdown,

a second ceramic substrate (12A) comprising:

a body having a lower side facing the solid state devices (Figures 2C, 2D) and an upper side,

a plurality of conductive pads (38) bonded to the upper surface of the body,

a plurality of conductive pads (48) bonded to the lower side of the body, at least one pad for each contact on the solid state devices, facing the solid state devices and connected to the conductive contacts of the solid state device through 40 and 36, and

a plurality of vias (44) (Figure 2A) connecting at least some of the conductive pads (36) on the lower surface to at least one of the conductive pads (40) on the upper side of the body,

a plurality of terminals (42RF) (Figure 2D) (Col. 8, lines 22 – 25) connected to conductive pads on the upper surface of the second ceramic substrate,

a strip line comprising an insulating body (50) (Col. 8, line 57), a first conductive strip (36) and a second conductive strip (36), the first conductive strip being connected to a conductive pad (38) on the first ceramic substrate (12), and the second conductive strip (36) being connected to a different conductive pad (38) on the first ceramic substrate (12), and

a first encapsulant (30) (Figure 2C) encapsulating the solid state devices between the first and second ceramic substrate.

Farnworth et al. do not disclose that the coefficients of thermal expansion (CTE) of substrates is matched to that of the solid state device. Farnworth et al. do disclose that the substrate comprises a ceramic (Col. 4, line 57). Pace discloses (Col. 4, lines 7 – 16) that ceramic materials such as aluminum nitride and aluminum oxide have thermal expansion characteristics closely matched to semiconductor devices. Hence, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine Pace with Farnworth et al. to obtain a packaged device with reduced thermal stress.

Additionally, Farnworth et al. do not disclose a first encapsulant having a coefficient of thermal expansion (CTE) matched to the CTE of at least one solid state device (silicon). Epoxy resins are known to have CTE values that are close to that of silicon. Hitachi Chemical, for example, produces an epoxy resin with CTE values[1] in the range, 6 to 38 x 10^(-6)/C, in a comparable range with silicon (4.2 x 10^(-6)/C). Hence, it would have been obvious to one of ordinary skill in the art at the time of the invention to use known CTE values to obtain approximately matching values for encapsulant and device to reduce the amount of thermally induced stress and damage.

4. Regarding Claims 4, 12, 22, and 23, Farnworth et al. discloses a second encapulant (30, top) (Figure 2D) covering all of the assembly except for the lower side of the first ceramic substrate and ends of the terminals (42RF), resulting in a "shell" covering.

5. Regarding Claims 5 and 13, Farnworth et al. discloses that the ceramic substrates (12, 12A)

1) Hitachi Chemical Co., "Epoxy Molding Compounds," (2003).

and the insulating cover layer (50) comprise a shell covering all of the assembly except for the lower side of the first ceramic substrate and ends of terminals (42RF) opposite the second ceramic substrate.

6. Regarding Claims 6 and 14, as discussed for Claim 4, Farnworth et al. disclose a second encapsulant (30, top) inside the shell.

7. Regarding Claims 8, 16, and 28, Farnworth et al. discloses (Col. 6, lines 12 – 14) at least one conductor (44) connecting a conducting pad on the first ceramic substrate (12) and a conductive pad on the second ceramic substrate (12A).

8. Regarding Claim 9, Farnworth et al. disclose a package for at least one solid state device comprising a body having a coefficient of thermal expansion and a plurality of conductive contacts, the package comprising:

a first ceramic substrate (12) and a second ceramic substrate (12A), spaced apart a sufficient distance for at least one solid state device (20, upper) to be located therebetween, the conductive contacts (34) on the solid state device (20) facing the second ceramic substrate (12A),

the first ceramic substrate comprising:

a body having a lower side and an upper side facing the solid state devices (Figure 2D),

a conductive pad (48) covering the lower side, and

one conductive pad (38) (Figure 2D) connected to each of the solid state devices packaged, each conductive pad (38) being bonded to the upper side of the body and connected to the solid state device with which it is associated, each pad being separated from other metal pads by a distance sufficient to prevent breakdown,

a second ceramic substrate (12A) comprising:

a body having a lower side facing the solid state devices (Figure 2D) and an upper side,

a plurality of conductive pads (38) bonded to the upper surface of the body,

a plurality of conductive pads (48) bonded to the lower side of the body, at least one pad for each contact on the solid state devices, facing the solid state devices and connected to the conductive contacts of the solid state device through 40 and 38, and

a plurality of vias (44) (Figure 2A) connecting at least some of the conductive pads (48) on the lower surface to at least one of the conductive pads (40) on the upper side of the body,

a plurality of terminals (42RF) (Figure 2D) (Col. 8, lines 22 – 25) connected to conductive pads on the upper surface of the second ceramic substrate,

a strip line (36) comprising an insulating body (50), a first conductive strip (36) and a second conductive strip (36), the first conductive strip being connected to a conductive pad (38) on the first ceramic substrate (12), and the second conductive strip (36) being connected to a different conductive pad (38) on the first ceramic substrate (12), and

such that when at least one solid state device is mounted in the package, the space between the first ceramic substrate (12) and the second ceramic substrate (12A) is filled with an

encapsulant (30), wherein the device is encapsulated.

Farnworth et al. do not disclose that the coefficient of thermal expansion (CTE) of the first and second substrate is matched to that of the solid state device. However, Farnworth et al. do disclose that the substrates are composed of ceramic (Col. 3, lines 30 – 32). However, Pace discloses (Col. 4, lines 7 – 16) that ceramic materials, such as aluminum nitride and aluminum oxide, have thermal expansion characteristics closely matched to semiconductor devices. Hence, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine Pace with Farnworth et al. to obtain a packaged device with reduced thermal stress.

In like fashion, Farnworth et al. do not disclose that the CTE of the first encapsulant is matched with the CTE of the at least one solid state device. Epoxy resins, as discussed above, are known to have CTE values that are close to that of silicon. Hitachi Chemical, for example, produces an epoxy resin with CTE values in the range, 6 to 27 x 10^(-6)/C, in a comparable range with silicon (4.2 x 10^(-6)/C). Hence, it would have been obvious to one of ordinary skill in the art at the time of the invention to use known CTE values to obtain approximately matching values for encapsulant and device to reduce the amount of thermally induced stress and damage.

9. Regarding Claim 17, Farnworth et al. disclose a method of packaging at least one solid state device, each solid state device comprising a body (silicon) (COL. 4, Line 60) having a CTE and a plurality of conductive contacts (34) (Figure 3) using a first ceramic substrate (12) and a

second ceramic substrate (12A), the method comprising the steps of:

providing a second ceramic substrate (12A) comprising:

a body having a CTE and a lower and upper side (Figure 2D),

a plurality of conductive pads (48) bonded to the upper surface of the body,

a plurality of conductive pads (38) bonded to the lower side of the body, at least one pad for each contact on the solid state devices, facing the solid state devices and connected to the conductive contacts of the solid state device, and

a plurality of vias (44) (Figure 2A) connecting at least some of the conductive pads (36) on the lower surface to at least one of the conductive pads (48) on the upper side of the body,

placing the solid state devices on the lower side (12c) of the second ceramic substrate, with contacts (34) of the solid state devices in alignment with conductive pads (38) on the lower side of the second ceramic substrate (Figure 3),

connecting the contacts (wire 28, Figure 3) of the solid state device to the conductive pads on the lower side of the second ceramic substrate,

assembling the connected solid state devices and second ceramic substrate (12A) with a first ceramic substrate (12) comprising:

a body having a lower side and an upper side facing the solid state devices (Figure 2D) (bottom of Figure 2D, facing device),

a conductive pad (38) covering the lower side, and

one conductive pad (38) (Figure 2D) connected to each of the solid state devices packaged, each conductive pad (38) being bonded to the upper side of the body and con-

nected to the solid state device with which it is associated, each pad being separated from other metal pads by a distance sufficient to prevent breakdown,

connecting the conductive pads (48) on the upper side of the first ceramic substrate to the solid state devices (Figures 2A, 2D),

connecting a plurality of terminals to the conductive pads (40) on the upper surface of the second ceramic substrate,

connecting a strip line (36) comprising an insulating body (12), a first conductive strip (36) and a second conductive strip (36) to conductive pads (40) on the first ceramic substrate and second ceramic substrate

filling the space between the first and second ceramic substrate with a first encapsulant (30) (Figure 2C) encapsulating the solid state devices using a mold (Col. 7, line 66 through Col. 8, line 3).

As discussed for Claim 1, Farnworth et al. do not disclose that the coefficient of thermal expansion of the first and second substrate is matched to that of the solid state device (silicon). However, Farnworth et al. do disclose that the substrates are composed of ceramic (Col. 3, lines 30 – 32). It is known from reference materials that the coefficient of thermal expansion of silicon and for a ceramic material such as aluminum nitride are comparable. It would have been obvious to one of ordinary skill in the art at the time of the invention to use known physical values of thermal expansion coefficients to obtain approximately matching values of ceramic and device (silicon) to reduce the amount of thermally induced stress and damage.

Additionally, Farnworth et al. do not disclose a first encapsulant having a coefficient of thermal

expansion (CTE) matched to the CTE of at least one solid state device (silicon). Epoxy resins are known to have CTE values that are close to that of silicon, as discussed in Claim 1.Hence, it would have been obvious to one of ordinary skill in the art at the time of the invention to use known CTE values to obtain approximately matching values for encapsulant and device to reduce the amount of thermally induced stress and damage.

10. Regarding Claim 19, Farnworth et al. disclaose a method comprising encapsulating the assembled upper side of the first substrate, second substrate, solid state devices, strip line, and terminals in a second encapsulant (30) (Col. 7, line 66 through Col. 8, line 17) using a mold (Col. 8, lines 1 and 2), leaving the lower side of the first ceramic substrate, an outer portion of each of the terminals and an outer portion of the strip line free of encapsulant (Figure 2D).

13. Claims 7, 15, and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Farnworth et al., as applied to Claims 1 – 6, 8 – 14, 16, 17, 19, 22, 23, and 28, and further in view of Nagesh et al. (US 5,155,661).

13. Regarding Claims 7, 15, and 27, Farnworth et al. do not disclose the presence of a heat sink coupled to the first ceramic substrate. Nagesh et al. disclose a heat sink (48) coupled to a ceramic substrate (14). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the heat sink of Nagesh et al. in Farnworth et al. to assist in heat reduction and lowering of stress at the substrate/device interface.

16. Claims 18, 20, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Farnworth et al., as applied to Claims 1 – 6, 8 – 14, 16, 17, 19, 22, 23, and 28, and further in view of Chen et al. ("Novel Packaging Structures, Encapsulation Process and Materials for Matrix Array Over-Molded Flip Chip CSP," Proc. Electronic Packaging Tech., (10 – 12 Dec., 2003), pp.141 – 144).

17. Regarding Claims 18, 20, and 21, Farnworth et al. do not disclose a method comprising the use of a vacuum molding procedure for encapsulating a solid state device. However, the use of vacuum molding is a widely applied technique in the art. Chen et al., for example, disclose the procedures for vacuum molding and encapsulation for a device structure. It would have been obvious to one of ordinary skill in the art at the time of the invention to use the procedures of Chen et al. in Farnworth et al. to obtain an encapsulated layer free of voids (Chen et al., Abstract, 2nd para.)

18. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Farnworth et al., as applied to Claims 1 – 6, 8 – 14, 16, 17, 19, 22, 23, and 28, and further in view of Kazama et al. (US 6,639,315 B2).

19. Regarding Claim 24, Farnworth et al. do not explicitly disclose a method (Col. 8, lines 19 – 31) in which the conductive pads on the first ceramic substrate and the contacts of the solid state device, the terminals and conductive pads on the second ceramic, and the conductive strips of the strip line and the conductive pads on first and second ceramic substrates are

connected by placing a layer of solder between each pad and contact and placing in a re-flow oven to melt the solder. Kasama et al, disclose a procedure wherein solder is placed on contacts and the wafer placed in a reflow oven to melt the solder (Col. 11, lines 42 – 45). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Farnworth et al. and Kasama et al. to obtain reliable solder connections.

18. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Farnworth et al., as applied to Claims1 – 6, 8 – 14, 16, 17, 19, 22, 23, and 28 and further in view of Canfield Technologies Technical Bull. No. 124, (2003).

19. Regarding Claim 25, Farnworth et al. do not disclose the step of cleaning to remove flux and debris after a solder/reflow process step. However, Canfield Technologies discloses that the debris and residue are removed with application of solvents (p. 2). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Canfield Technologies Bulletin and Farnworth et al. to provide surfaces free of debris and/or impurities.

20. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Farnworth et al., in view of Kazama et al., as applied to Claims 1 – 6, 8 – 14, 16, 17, 19, 22, 23, and 28, and further in view of Nguyen (US 5,973,932).

21. Regarding Claim 26, Farnworth et al. do not explicitly disclose the step of temperature and environment to reduce stress. Nguyen discloses the use of a solder alloy, wherein the temper-

ature is controlled to melt the solder (Col. 5, line 63 through Col. 6, line 7) and reduce stress (Col. 2, lines 43 – 46). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Farnworth et al. and Nguyen to obtain reliable solder connections.

Conclusions

22. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to **Thomas Magee**, whose telephone number is **(571) 272 1658.** The Examiner can normally be reached on Monday through Friday from 8:30AM to 5:00PM (EST). If attempts to reach the Examiner by telephone are unsuccessful, the examiner's supervisor, **Eddie Lee**, can be reached on **(571) 272-1732.** The fax number for the organization where this application or proceeding is assigned is **(703) 872-9306.**

EDDIE LEE
SUPERVISORY PATENT EXAMINER
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Thomas Magee
March 30, 2005